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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/937,877    09/29/97    TSYRGANOVICH    A    ZILG-183US0

LM02/0927

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EXAMINER

SRIVASTAVA, V

ART UNIT

PAPER NUMBER

2711

4

DATE MAILED: 09/27/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

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File Copy

# Office Action Summary

Application No.  
**08/937,877**

Applicant(s)  
**Anatoliy V. Tsyrganovich**

Examiner  
**Vivek Srivastava**

Group Art Unit  
**2711**



☐ Responsive to communication(s) filed on \_\_\_\_\_

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claims

☒ Claim(s) 1-29 is/are pending in the application.

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

☒ Claim(s) 12 is/are allowed.

☒ Claim(s) 1-3, 6-9, 11, 13-25, and 27-29 is/are rejected.

☒ Claim(s) 4, 5, 10, and 26 is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☐ None of the CERTIFIED copies of the priority documents have been  
☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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## DETAILED ACTION

### *Claim Rejections - 35 U.S.C. § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 - 3, 6, 8, 9, 11, 13, 14 - 19, 25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al.

Considering claim 1, Kobayashi discloses a first circuit portion with a delay element (fig 5 item 22), a second circuit portion coupled to the first circuit portion including a delayed input (fig 5 item 26), an adjustment input not passing through the delay element (fig 5 item 27), wherein with no adjustment input the circuit acts as a filter (fig 5, when no adjusting is required and K1 and K2 equal to one, the circuit acts like a filter), and wherein an adjustment input changes the level of the output (fig 5 adjustments coefficients K2 and K1 will change the level of output Dvec).

Considering claim 2, Kobayashi discloses the first circuit portion is a delay line (see fig 5 item 22).

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Considering claim 3, Kobayashi discloses a second circuit which includes at least one coefficient circuit connected to one of the at least one delayed signal inputs and to the adjustment input (see fig 5, second circuit, or coefficient circuit item 26 is connected to a delayed input and to adjustment input).

Considering claim 6, Kobayashi discloses a summer circuit to add the outputs of the coefficient circuit (fig 5 items 25 and 26, the circuit in claim 3/1 is assumed since applicant does not claim the second circuit).

Considering claim 8, Kobayashi discloses a differential phase input (see fig 5, differential phase input  $Do(N+1)$  is input to delay circuit).

Considering claim 9, Kobayashi inherently discloses the adjustment control logic adapted to provide the adjustment input (fig 5, col 4 lines 23 - 68).

Considering claim 11, Kobayashi discloses a second circuit portion which acts as a filter to the first input when there is not adjustment input (see fig 5, when no adjustment input is provided to circuit 26, the circuit functions as a filter).

Considering claim 13, Kobayashi discloses the claimed providing a circuit, inputting an input signal into the circuit such that the circuit filters the input signal to provide a filtered component to the output of the circuit (fig 5 items 21 and 22) and inputting an adjustment signal into the circuit so that the adjustment signal provides an unfiltered offset to the output (fig 5 adjustments coefficients  $K2$  and  $K1$  will change the level of output  $Dvec$ ).

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Considering claim 14, Kobayashi inherently discloses wherein the adjustment signal keeps the output within a preset range (col 4 lines 23 - 68, adjustment signal must keep output in a preset range in order to maintain a correct output).

Considering claims 15 and 19, Kobayashi discloses filtering of the input signal is a low-pass filtering (see frequency response in fig 6C from time  $t_0 - t$ ).

Considering claim 16, Kobayashi discloses the claimed wherein the input is a phase signal (col 4 lines 24 - 59).

Considering claims 17 and 27, Kobayashi discloses wherein the input is a hue signal (col 1 lines 7 - 11).

Considering claims 18 and 28, Kobayashi inherently discloses constraining a phase signal within a preset range (in order to adjust correct the phase, the output phase must be inherently constrained within a preset range), the constraining step including adding a correction signal to the phase signal (fig 5), filtering the phase signal without filtering the correction signal portion of the phase signal (fig 5, when no adjusting is required, resulting in  $K_2$  and  $K_1$  equal to one, the circuits acts like a filter).

Considering claim 25, Kobayashi discloses wherein the constraining step is such that the phase signal is processed so as to use a differential input (see fig 5, differential phase input  $Do(N+1)$  is input to delay circuit).

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*Claim Rejections - 35 U.S.C. § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 21 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al.

Considering claim 21, Kobayashi inherently discloses a preset range (claim 18) but fails to disclose the claimed preset range of zero to  $2\pi$ .

The Examiner Takes Official Notice it would have been well known in the television art to keep the phase within a range of zero to 180 deg ( $2\pi$ ) to prevent overlapping with components in another phase range resulting in color distortion. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kobayashi to include the claimed preset range to prevent overlapping of components in different phases resulting in picture color distortion.

Considering claim 22, Kobayashi inherently discloses a preset range (claim 18) but fails to disclose the preset range is zero to  $2\pi$  plus a guard band.

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The Examiner Takes Official Notice it would have been well known in the television art to keep the phase within a range of zero to  $180^\circ$  ( $2\pi$ ) to prevent overlapping with data in another phase range resulting in color distortion. Furthermore, it would have been well known in the television art to include a guard band to prevent interference from overlapping phases. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kobayashi to include the claimed preset range plus guardband to prevent overlapping of phases resulting in picture color distortion and interference.

Considering claim 23, Kobayashi fails to disclose wherein the guard band is a reference value above or below the range zero to  $2\pi$ .

It would have been obvious to include a guard band in Kobayashi (claim 22). Furthermore, it would have been obvious to include the reference guard band above or below the range zero to  $2\pi$  to prevent overlapping of phases resulting interference. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Kobayashi to include the claimed guard band to prevent the overlapping of phases resulting in interference.

Considering claim 24, Kobayashi fails to disclose wherein the guard bands are  $-\pi$  to zero and  $2\pi$  to  $3\pi$ .

It would have been obvious to include guard bands in Kobayashi (claim 22). It would have been obvious including guard bands between the range of  $-90^\circ$  ( $-\pi$ ) to zero and  $180^\circ$  ( $2\pi$ ) to  $270^\circ$  ( $3\pi$ ) would secure the range of 0 to  $180^\circ$  ( $2\pi$ ) by preventing the overlapping

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of phases resulting in interference. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the claimed guard bands to prevent the overlapping of phases resulting in interference.

5. Claims 7, 20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al in view of Namiki et al.

Considering claim 7, Kobayashi discloses wherein the first input and output are phase representations but fails to disclose an adjustment input causes an integer multiple of 180 deg (2pi) shift in the output signal.

Kobayashi discloses adjusting and converting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include shifting the phase by 180 deg or (2pi) to prevent color distortion in the displayed video signal.

Considering claim 20, Kobayashi fails to disclose wherein the correction signal is an integer multiple of 2pi.

Kobayashi discloses adjusting and converting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. Therefore, it would have been obvious to one having ordinary skill in the art at the



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time the invention was made to include shifting the phase by 180 deg or (2pi) to prevent color distortion in the displayed video signal.

Considering claim 29, Kobayashi discloses providing picture data including hue information encoded as phase having a first range (col 1 lines 5 - 11, col 4 lines 24 - 68, phase includes hue data encoded in a first phase range) and producing a filtered hue information signal with unfiltered offsets (fig 5, when no adjusting is required, K2 and K1 offsets are not filtered). Hue fails to disclose offsets of plus or minus 2pi.

Kobayashi discloses adjusting and correcting the phase of a signal. Namiki teaches by shifting the phase by 180 deg (2pi) color distortion in a displayed television signal can be prevented. It would have been obvious shifting the phase plus or minus 2pi, or shifting the phase 180 deg would have provide phase correction thus preventing color distortion. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include shifting the phase by plus or minus 180 deg or (2pi) to prevent color distortion in the displayed video signal.

***Allowable Subject Matter***

6. Claims 4, 5, 10, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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7. Claim 12 is allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach a circuit comprising a digital filter, coefficient multiplier circuitry adapted to multiply the signal values by filter coefficients, and a summer connected to the coefficient multiplier circuitry to produce and output value wherein the summing circuitry is connected to the input lines of the signal values at different time indexes and to an adjustment input and the output of the summing circuitry is sent to a coefficient multiplying circuitry.

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Isono et al (4,197,556) - Hue correction circuit

Sanada et al (4,091,411) - Color hue control circuit

Nakagawa et al (4,644,389) - Digital television signal processing circuit

Ekstrand (3,688,021) - Tint control

Yoshinaka et al (4,714,954) - Read start pulse generator for time base corrector

Kosaka et al (4,939,572) - Video signal processing apparatus

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**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

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**or faxed to:**

(703) 308-9051, (for formal communications intended for entry)

**Or:**

(703) 308- 5399 (for informal or draft communications, please label


"PROPOSED" or "DRAFT")


Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vivek Srivastava whose telephone number is (703) 305 - 4038. The examiner can normally be reached on Monday - Thursday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andy Faile, can be reached at (703) 305 - 4380.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 305 - 3900.

  
VS 9/25/00

  
ANDREW I. FAILE  
SUPERVISORY PATENT EXAMINER  
GROUP 2700